FIG. 1

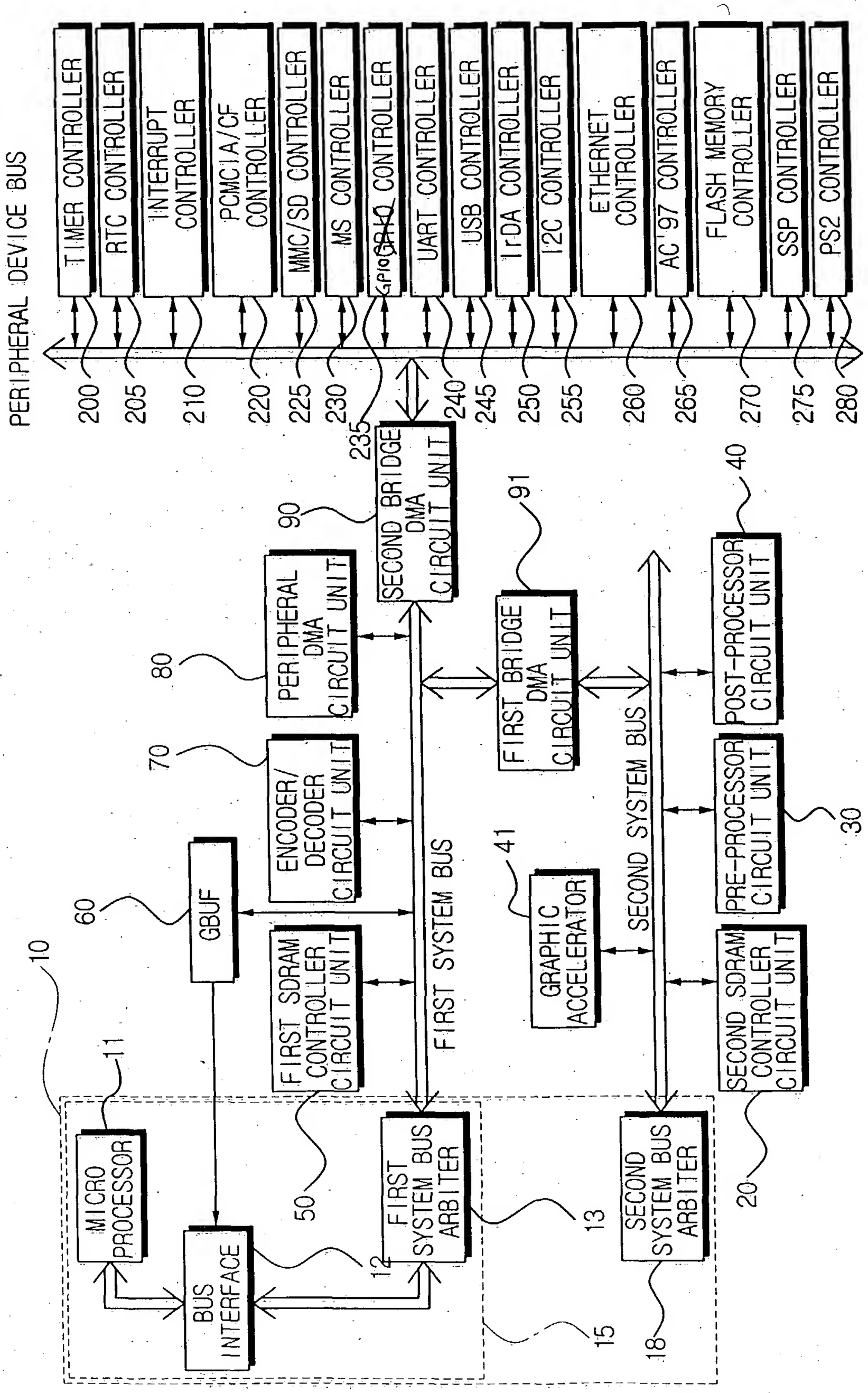
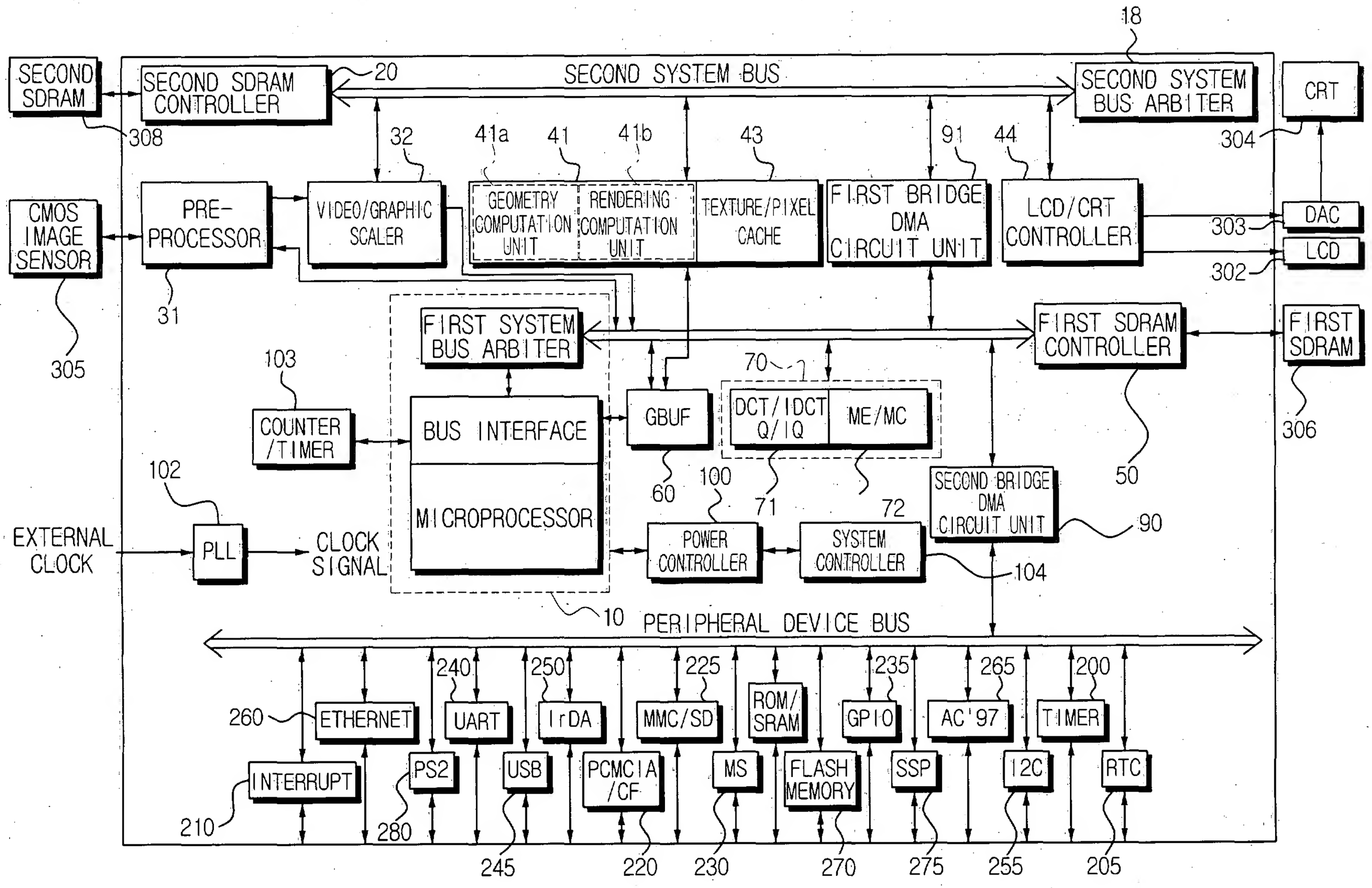

PERIPHERAL DEVICE BUS
TIMER CONTROLLER
RTC CONTROLLER
INTERRUPT CONTROLLER
PCMCIA/CF CONTROLLER
MMC/SD CONTROLLER
MS CONTROLLER
GPIO CONTROLLER
UART CONTROLLER
USB CONTROLLER
IrDA CONTROLLER
I2C CONTROLLER
ETHERNET CONTROLLER
AC'97 CONTROLLER
FLASH MEMORY CONTROLLER
SSP CONTROLLER
PS2 CONTROLLER
200
205
210
220
225
230
235
240
245
250
255
260
265
270
275
280
SECOND BRIDGE DMA CIRCUIT UNIT
90
PERIPHERAL DMA CIRCUIT UNIT
80
ENCODER/ DECODER CIRCUIT UNIT
70
FIRST BRIDGE DMA CIRCUIT UNIT
91
40
POST-PROCESSOR CIRCUIT UNIT
PRE-PROCESSOR CIRCUIT UNIT
30
SECOND SYSTEM BUS
FIRST SYSTEM BUS
GBUF
60
FIRST SDRAM CONTROLLER CIRCUIT UNIT
50
GRAPHIC ACCELERATOR
41
SECOND SDRAM CONTROLLER CIRCUIT UNIT
20
10
11
MICRO PROCESSOR
BUS INTERFACE
12
FIRST SYSTEM BUS ARBITER
13
SECOND SYSTEM BUS ARBITER
15
18

FIG. 2



Jae-hyun KIM
SYSTEM ON-A-CHIP PROCESSOR.....
Daryl Mexic
August 5, 2003
2 of 2
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